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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/791,096
Filing Date: March 01, 2004
Appellant(s): RYAN ET AL.

William D. Zahrt II
Registration No. 26,070
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/11/2006 appealing from the Office action mailed 3/11/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

Claims 1, 2, and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) as applied to claim 6 above, and further in view of Tseng (U.S. 2005/0035460).

Claims 11, 12, 15-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) and Tseng (U.S. 2005/0035460).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

Claim Rejections - 35 USC § 103

Claims 1, 2, and 4-7 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929).

Regarding claim 1, Chang teaches a method of forming an integrated circuit comprising providing a semiconductor substrate (**200** in Fig. 2D); forming a gate dielectric on the semiconductor substrate (**206** in Fig. 2D; column 3, lines 36-39); forming a gate on the gate dielectric (**208** in Fig. 2D; column 3, lines 46-47); forming source/drain junctions in the semiconductor substrate (**210** in Fig. 2D; column 3, line 59- column 4, line 39); and forming a nickel silicide on the source/drain junctions and on the gate (**234** in Fig. 2G; column 4, line 56 – column 5, line 10) within a thermal budget having a temperature dependent upon a silicide metal (the instant application on p. 9, lines 23-24 discloses that the thermal budget for nickel silicides is about 400 °C to 450 °C; Chang discloses forming the silicide at a temperature of about 400 to 800 °C, overlapping with the entirety of the thermal budget of nickel silicides).

Chang does not teach depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes within the thermal budget for forming the silicide; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming contact liners in the contact

holes within the thermal budget for forming the silicide (tungsten nitride, paragraph 0021; Lin discloses keeping the reaction chamber at a temperature between 250 °C and 550 °C, a temperature range that overlaps with the thermal budget of nickel silicides); and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts (tungsten, paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of tungsten nitride and the contacts are formed of tungsten, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Regarding claim 2, Chang and Lim together teach the method of claim 1. Lim further teaches that forming the contact liners uses an atomic layer deposition process (paragraph 0021).

Regarding claim 4, Chang and Lim together teach the method of claims 1 and 11. Chang further teaches that forming the silicide forms a nickel silicide (column 4, line 56 – column 5, line 10).

Regarding claim 5, Chang and Lim together teach the method of claim 1 and 11. Lim further teaches that forming the contacts forms a tungsten material (paragraph

0026); and forming the contact liners forms a tungsten nitride material (paragraph 0021).

Regarding claim 6, Chang teaches a method of forming an integrated circuit comprising providing a semiconductor substrate (**200** in Fig. 2D); forming a gate dielectric on the semiconductor substrate (**206** in Fig. 2D; column 3, lines 36-39); forming a gate on the gate dielectric (**208** in Fig. 2D; column 3, lines 46-47); forming source/drain junctions in the semiconductor substrate (**210** in Fig. 2D; column 3, line 59- column 4, line 39); and forming a nickel silicide on the source/drain junctions and on the gate (**234** in Fig. 2G; column 4, line 56 – column 5, line 10) within a thermal budget having a temperature of less than about 400 degrees centigrade (Chang teaches forming the silicide at a temperature of about 400 °C to 800 °C, which overlaps with the claimed temperature range at about 400 °C, and since the claimed temperature range "less than about 400 degrees centigrade" is not specific, it could be interpreted as, for example, "less than 402 degrees centigrade," which Chang teaches).

Chang does not teach depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming tungsten nitride contact liners in the contact holes within the thermal budget for forming the nickel silicide; and forming tungsten contacts in the contact holes over the contact liners.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming tungsten nitride contact liners in the contact holes (paragraph 0021) within the thermal budget for forming the silicide (Lin discloses keeping the reaction chamber at a temperature between 250 °C and 550

°C, a temperature range that overlaps with the thermal budget of nickel silicides); and forming tungsten contacts in the contact holes over the contact liners (paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming tungsten nitride contact liners in the contact holes; and forming tungsten contacts in the contact holes over the contact liners, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Regarding claim 7, Chang and Lim together teach the method of claim 6. Lim further teaches that forming the tungsten nitride liners uses an atomic layer deposition process (paragraph 0021).

Claim 9 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) as applied to claim 6 above, and further in view of Tseng (U.S. 2005/0035460).

Regarding claim 9, Chang and Lim together teach the method of claim 6 (note 35 U.S.C. 103(a) rejection above), but do not teach that forming the nickel silicide uses an ultra-thin thickness of a nickel silicide metal.

Tseng teaches forming nickel silicide layers with a thickness of 50 – 350 Å (paragraph 0037), within the limits indicated in the instant specification on page 8, line 4 of "not more than 50 Å thickness."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and taught by claim 6, and further make the nickel silicide layer ultra-thin, as taught by Tseng. The motivation for doing so at the time of the invention would have been to provide a semiconductor device with reduced contact resistance, as taught by Tseng (paragraph 0009).

Claims 11, 12, 15-17, and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) and Tseng (U.S. 2005/0035460).

Regarding claim 11, Chang teaches an integrated circuit comprising a semiconductor substrate (**200** in Fig. 2D); a gate dielectric on the semiconductor substrate (**206** in Fig. 2D; column 3, lines 36-39); a gate on the gate dielectric (**208** in Fig. 2D; column 3, lines 46-47); source/drain junctions in the semiconductor substrate (**210** in Fig. 2D; column 3, line 59-column 4, line 39); and a nickel silicide on the source/drain junctions and on the gate (**234** in Fig. 2G; column 4, line 56 – column 5, line 10).

Chang does not teach an interlayer dielectric having contact holes therein above the semiconductor substrate; contact liners in the contact holes; and contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts. Chang also does not teach that the silicide is an ultra-thin silicide.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts (tungsten, paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of tungsten nitride and the contacts are formed of tungsten, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Additionally, Tseng teaches forming nickel silicide layers with a thickness of 50 – 350 Å (paragraph 0037), within the limits indicated in the instant specification on page 8, line 4 of "not more than 50 Å thickness."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and further make the nickel silicide layer ultra-thin, as taught by Tseng. The motivation for doing so at the time of the invention would have

been to provide a semiconductor device with reduced contact resistance, as taught by Tseng (paragraph 0009).

Regarding claim 12, Chang, Lim, and Tseng together teach the integrated circuit as claimed in claim 11. Chang further teaches that the silicide is a nickel silicide (column 4, line 56 – column 5, line 10).

Regarding claim 15, Chang, Lim, and Tseng together teach the integrated circuit as claimed in claim 11. Lim further teaches that the contacts in the contact holes are tungsten (paragraph 0026).

Regarding claim 16, Chang, Lim, and Tseng together teach the integrated circuit as claimed in claim 11. Lim further teaches that the contacts are a tungsten material (paragraph 0026) and the contact liners are a tungsten nitride material (paragraph 0021).

Regarding claim 17, Chang teaches an integrated circuit comprising a semiconductor substrate (**200** in Fig. 2D); a gate dielectric on the semiconductor substrate (**206** in Fig. 2D; column 3, lines 36-39); a gate on the gate dielectric (**208** in Fig. 2D; column 3, lines 46-47); source/drain junctions in the semiconductor substrate (**210** in Fig. 2D; column 3, line 59-column 4, line 39); and a nickel silicide on the source/drain junctions and on the gate (**234** in Fig. 2G; column 4, line 56 – column 5, line 10).

Chang does not teach an interlayer dielectric having contact holes therein above the semiconductor substrate; tungsten nitride contact liners in the contact holes; and

tungsten contacts in the contact holes over the contact liners. Chang also does not teach that the silicide is an ultra-thin silicide.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming tungsten nitride contact liners in the contact holes; and forming tungsten contacts in the contact holes over the contact liners (tungsten, paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming tungsten nitride contact liners in the contact holes; and forming tungsten contacts in the contact holes over the contact liners, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Additionally, Tseng teaches forming nickel silicide layers with a thickness of 50 – 350 Å (paragraph 0037), within the limits indicated in the instant specification on page 8, line 4 of "not more than 50 Å thickness."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and further make the nickel silicide layer ultra-thin, as taught by Tseng. The motivation for doing so at the time of the invention would have

been to provide a semiconductor device with reduced contact resistance, as taught by Tseng (paragraph 0009).

Regarding claim 20, Chang, Lim, and Tseng together teach the method of claim 17. Chang further teaches that the gate and source and drain regions are ion-implanted with arsenic prior to the formation of nickel silicide on the gate and source and drain regions, so the nickel silicide further comprises arsenic doping (column 4, lines 23-39).

Claim 10 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) as applied to claims 6 above, and further in view of Tseng (U.S. 2005/0035460) and Wolf et al. (*Silicon Processing for the VLSI Era*, Vol. 1).

Regarding claim 10, Chang and Lim together teach the method of claim 6 (note 35 U.S.C. 103(a) rejections above), but do not teach that the interlayer dielectric is a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

Tseng teaches an interlayer dielectric made of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants (120 in Fig. 1; paragraph 0038).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and taught by claim 6, and further make the interlayer dielectric of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants, as taught by Tseng. The motivation for

doing so at the time of the invention would have been to keep capacitance between metallization layers low, as taught by Wolf et al. (line 1 of Table 15.4, pg. 727).

Claims 14 and 19 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) and Tseng (U.S. 2005/0035460) as applied to claims 11 and 17 above, and further in view of Wolf et al. (*Silicon Processing for the VLSI Era*, Vol. 1).

Regarding claims 14 and 19, Chang, Lim, and Tseng together teach the device of claims 11 and 17 (note 35 U.S.C. 103(a) rejection above).

Tseng additionally teaches an interlayer dielectric made of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants (120 in Fig. 1; paragraph 0038).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate the integrated circuit taught by Chang, Lim, and Tseng together, and also taught by claims 11 and 17, and further make the interlayer dielectric of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants, as taught by Tseng. The motivation for doing so at the time of the invention would have been to keep capacitance between metallization layers low, as taught by Wolf et al. (line 1 of Table 15.4, pg. 727).

(10) Response to Argument

Issue #1 (as identified by Appellants):

Regarding claims 1, 2, and 4-5, Appellants argue that Chang (U.S. 6,858,506) teaches away from Appellants' invention as claimed because Chang teaches forming a metal silicide layer by annealing at a temperature of about 400 to 800 degrees Celsius (Chang, column 4, lines 60-66), which includes temperatures above those disclosed by Appellants to be within the thermal budget for nickel silicide (400 – 450 degrees Celsius; instant specification, p. 9, lines 23-24). Appellants argue that by teaching a high range of anneal temperatures, Chang indicates that the thermal budget of the silicide is not critical, and therefore teaches away from the instant invention (Appellants' arguments, pp. 11-12, specifically the second full paragraph on p. 12).

However, this argument is not persuasive because the temperature range to form a silicide taught by Chang (400 to 800 °C) includes the range 400 to 450 °C, which Applicant discloses is the thermal budget for nickel silicide.

It has been held that "in the case where the claimed ranges 'overlap or lie inside ranges disclosed by the prior Art' a prima facie case of obviousness exists." *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.); *In re Geisler*, 116 F.3d 1465, 1469-71, 43 USPQ2d 1362, 1365-66 (Fed. Cir. 1997) (Claim reciting thickness of a protective layer as falling within a range of "50

to 100 Angstroms" considered prima facie obvious in view of prior art reference teaching that "for suitable protection, the thickness of the protective layer should be not less than about 10 nm [i.e., 100 Angstroms]." The court stated that "by stating that suitable protection' is provided if the protective layer is about' 100 Angstroms thick, [the prior art reference] directly teaches the use of a thickness within [applicant's] claimed range.").

Chang may be silent regarding the motivation for forming the silicide within a particular temperature range, but does teach using a temperature within the range disclosed by Applicant to be within the thermal budget for nickel silicide.

Moreover, as defined by Appellants, a thermal budget is "the cumulative number of degrees of temperature than an integrated circuit can be subjected to during its various manufacturing processes before excess dopant migration occurs and an integrated circuit will no longer function properly" (Appeal Brief, p. 12, second full paragraph). However, in claim 1, Appellants do not claim a specific temperature range for the thermal budget. Any teaching of forming a metal silicide on an integrated circuit that functions properly necessarily teaches, and therefore reads on, the limitation of forming the silicide "within a thermal budget having a temperature dependent upon a silicide metal," taking the definition of thermal budget supplied by Appellants.

Appellants further argue that "the Chang teaching away is even clearer because the claim limitations require both the silicide and the contact liners to be formed within the thermal budget for forming the silicide alone" (Appeal Brief, p. 12, third full paragraph).

However, Chang's not teaching the formation of contact liners does not constitute teaching away from Appellants' invention. Forming an interlayer dielectric with contact holes and contact liners in the contact holes are process steps well known in the art of semiconductor processing as a means of providing and accessing electrical signals to and from devices on an integrated circuit. The secondary reference, Lim (U.S. 2004/0115929), teaches a simplified method of forming contact liners (barrier metal layers) that improves the step coverage of the barrier metal layer at a fine contact hole (Lim, paragraph 0014), so there is motivation to combine the teachings of Chang and Lim, as detailed in section (9) above. Furthermore, Lim teaches forming the contact liner at a temperature range between 250 °C and 550 °C, a range that overlaps with Appellants' disclosed thermal budget for forming nickel silicide. In claim 1, Appellants do not claim a temperature range or a processing time associated with any temperature range, and both the silicide taught by Chang and the contact liner taught by Lim are formed within temperature ranges that overlap with the temperature range disclosed by Appellant to be within the thermal budget for nickel silicide. Therefore, neither Chang alone nor the combined teachings of Chang and Lim teaches away from Appellants' invention as claimed in claim 1.

Appellants further argue that the combination of references does not even mention all of the claim limitations (Appeal Brief, p. 13, second full paragraph). However, the examiner has addressed every claim limitation in the final rejection dated 12/13/2005 and in section (9) above, and therefore does not find this argument

persuasive. Neither Chang nor Lim individually teaches all of the claim limitations, but the combination of references does.

Appellants additionally argue that "the references as a whole teach away from each other" and quote *In re Gordon* to support their argument that Chang and Lim can therefore not serve to create a prima facie case of obviousness (p. 13, third full paragraph).

However, as detailed above, neither Chang alone nor the combination of Chang and Lim teaches away from Appellants' invention. Furthermore, Chang and Lim do not teach away from each other. Chang does not disclose that further processing steps such as forming a contact liner would destroy the functionality of the transistor, and Lim does not disclose that the semiconductor substrate receiving an interlayer dielectric, contact liner (barrier metal), and contacts should not also comprise a metal silicide layer. Even in the context of claim 1, Chang and Lim do not teach away from each other. Claim 1 does not include the limitation that the processing time multiplied by the processing temperature for the combined formation of the metal silicide and contact liners does not exceed the thermal budget for the metal silicide. Rather, claim 1 includes the individual limitations of (a) forming the silicide within a thermal budget having a temperature dependent upon a silicide metal, and (b) forming contact liners within the thermal budget for forming the silicide. Chang teaches (a), Lim teaches (b), and there is motivation to combine these references.

Regarding claims 2 and 4-5, Appellants argue only that these claims depend upon claim 1 and are believed to be allowable for the same reasons that claim 1 is

allowable. The examiner does not believe these claims are allowable for the reasons detailed in section (9) above.

Regarding claim 6, Appellants argue that Chang teaches forming a silicide at a temperature greater than that claimed, and therefore teaches away from Appellants' invention (p. 14, paragraphs 2 and 3).

However, Chang teaches forming the silicide using a temperature range that overlaps with the range claimed by Appellants in claim 6 (see above response regarding claim 1). Therefore, Chang does not teach away from Appellants' invention.

Appellants continue to argue that since Chang does not teach forming "contact liners of any type in the contact holes, much less at the thermal budget claimed by Appellants," Chang teaches away from Appellants' invention (p. 14, paragraphs 4-6). Appellants additionally argue that since Lim "does not teach, suggest, or even mention the formation of any silicide within the thermal budget claimed by Appellants," Lim "fails to teach or suggest Appellants' invention as claimed..." (p. 15, first paragraph).

However, this argument is unpersuasive in the context of claim 6 for the reason given above in the context of claim 1. Claim 6 is different from claim 1 because it does claim a temperature range (less than about 400 degrees centigrade), but it still does not include the limitation that the *combined process* of forming the metal silicide and forming the contact liners must subject the integrated circuit to temperatures no greater than 400 degrees centigrade over some period of time. It is reasonable to interpret claim 6 as it is presently written that the *individual* process of forming the nickel silicide must occur at a temperature of less than about 400 degrees centigrade (and Chang

teaches a temperature range that overlaps with this claimed range), and the individual process of forming the contact line must occur at a temperature of less than about 400 degrees centigrade (and Lim teaches a temperature range that overlaps with this claimed range).

Regarding claim 7, Appellants argue only that this claim depends upon claim 6 and is believed to be allowable for the same reason that claim 6 is allowable. The examiner does not believe that this claim is allowable for the reasons detailed in section (9) above.

Regarding claims 11, Appellants argue that "the Examiner has stated the same rejection with regard to claim 1 above" (p. 15, paragraph 5), and submits that claim 11 is allowable over Chang in view of Lim taken either singly or in combination..." (p. 15, paragraph 7).

However in the final rejection dated 12/13/2005 and in section (9) above, the Examiner has additionally relied on the teachings of Tseng (U.S. 2005/0035460) to provide the limitation of an "ultra-thin" silicide (final rejection, p. 6, paragraph 4 – p. 8, paragraph 1). In the section of the Appeal Brief titled "Issue #1," Appellants do not address the combined teachings of Chang, Lim, and Tseng as they were applied to claim 11, and assert only that claim 11 is allowable over Chang in view of Lim.

Regarding claims 12, 15, and 16, Appellants argue that these claims depend upon claim 11 and are believed to be allowable for the same reasons that claim 11 is allowable. The examiner does not believe that these claims are allowable for the reasons detailed in section (9) above.

Similarly, Appellants argue (p. 16, paragraphs 1-5) regarding claim 17 that Chang does not mention the thickness of the silicide and that Lim does not teach a silicide, much less an ultra-thin silicide, so these claims are allowable over Chang in view of Lim.

However, the Examiner has additionally relied upon the teachings of Tseng to provide this limitation (see final rejection and section (9) above).

Regarding claim 20, Appellants argue that this claim depends upon claim 11 and is believed to be allowable for the same reasons that claim 11 is allowable. The examiner does not believe that claim 20 is allowable for the reasons detailed in section (9) above.

Issue #2 (as identified by Appellants):

Regarding claims 9, 11, and 17 (claims 13 and 18 were cancelled in the amendment dated 10/11/2005), Appellants argue that Chang and Lim, taken either singly or in combination, fail to teach or suggest forming an ultra-thin silicide (p. 17, second full paragraph), and that Tseng teaches away from Appellants' invention by disclosing silicides having a thickness greater than the claimed thickness (p. 17, paragraph 5). Appellants further argue that they have shown criticality in their specification regarding the thickness of the silicide layer, and that as a result, the examiner's combination of Chang, Lim, and Tseng is improper (paragraph bridging pp. 17 and 18).

However, this argument is not persuasive for two reasons. First, Tseng does not teach away from Appellants' invention by suggesting forming a silicide thicker than 50

Å, since Tseng also suggests forming a silicide with a thickness of 50 Å. Second, Appellants never claim a silicide thickness of 50 Å. Rather, Appellants claim an "ultra-thin" silicide, a broad term that does not have standard meaning in the art of semiconductor processing. Appellants disclose that "it is *preferable* that the silicide be deposited...to an ultra-thin thickness of not more than 50 Å thickness in order to provide an ultra-uniform, ultra-thin silicide" (instant specification, p. 9, lines 3-5, emphasis added). Appellants do not disclose that for the purposes of patentability, the term "ultra-thin" is defined to be not more than 50 Å. Since Tseng teaches forming a silicide layer with a thickness as low as 50 Å, the examiner considers this silicide ultra-thin, in the absence of any specific definition or claimed limitation.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Heather Doty

Conferees: Heather Doty, Carl Whitehead, Jr., Ricky Mack